REMARKS

Applicant respectfully requests reconsideration of the present application in view of the reasons that follow.

No claims have been amended. Claims 1-6 remain pending, of which claims 5-6 are withdrawn from consideration.

Rejection under 35 U.S.C. § 102

Claims 1-4 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,556,501 to Naffziger ("Naffziger"). Applicant respectfully traverses this rejection for at least the following reasons.

Independent claim 1 is directed to a register file and recites "said input port selector including a combinational circuit including a plurality of first AND gates each corresponding to one of said input ports and a first OR gate for generating a logical sum of outputs from said first AND gates, wherein: each of said first AND gates in one of said input port selector receives a write instruction signal for specifying whether or not write data input through a corresponding one of said input ports is to be stored in a corresponding one of said registers, and generates a logical product of said write data and said write instruction signal and an inverted signal of each of said write instruction signals received through said input ports each having a higher priority order compared to said input port corresponding to said one of said input port selector." Naffziger fails to disclose at least this feature of claim 1.

Naffziger discloses a multi-port computer register file which has shared word lines for read and write ports and storage elements that power down during write operations (abstract). FIG 4A of Naffziger illustrates circuitry for writing to bit 0 at write ports 6 and 7, and to read from bit 0 at read ports 6 and 9. The circuitry includes a direction line WR that is driven high during write operations.

Naffziger, however, discloses a completely different circuit structure from that recited in claim 1. While the circuitry of Naffziger includes AND gates 62, there do not appear to be

any OR gates "for generating a logical sum of outputs from said first AND gates" as recited in claim 1. Nor are the AND gates arranged to generate a logical product of (1) "said write data" and (2) "said write instruction signal" and (3) "an inverted signal of each of said write instruction signals received through said input ports each having a higher priority order compared to said input port corresponding to said one of said input port selector" as recited in claim 1. This is necessarily so because the AND gates 62 have only two inputs, one from a read/write port and another being the direction line WR. In particular, Naffziger does not disclose any AND gate which generates a logical product of inputs where one of the inputs is "an inverted signal of each of said write instruction signals received through said input ports each having a higher priority order compared to said input port corresponding to said one of said input port selector."

Furthermore, the first AND gates in claim 1 are arranged so as to generate "a logical product of said write data and said write instruction signal and an inverted signal of each of said write instruction signals received through said input ports each having a higher priority order compared to said input port corresponding to said one of said input port selector." In this configuration a priority order is specified for the plurality of AND gates, whereby only the AND gate specified by the write instruction signal and the priority order is activated to thereby reduce the power dissipation of the register file. Naffziger does not suggest this recited configuration. Naffziger discloses in col. 5 and FIG. 4A, that AND gate 66 receives an NWR signal which is an inversion signal of the direction line WR corresponding to Port 6, and outputs a logical product of the NWR signal and Read/Write Port 6 Word Line. Naffziger recites the relationship between Port 6 and the other Ports as: "Each port requires 7 bits to select a register, and there are 20 ports (12 read ports and 8 write ports)" (col. 5, lines 45-46), "Each port is 64 bits wide and there are 8 write ports" (col. 5, lines 49-50), and "Each port is 64 bits wide and there are 12 read ports" (col. 5, lines 53-54). Nowhere does Naffziger disclose or suggest, however, that Port 6 has a higher order as compared to the other ports, and thus does not specify a higher priority order as recited in claim 1.

Moreover, the Office Action cites generally to Naffziger as disclosing the features of claim 1, but fails to specifically identify the components in Naffziger corresponding to the

AND gates, OR gates, or the components of the logical product as recited in claim 1. If the Examiner maintains the rejection of the claims over Naffziger, the Examiner is respectfully requested to specifically identify these features of claim 1.

The dependent claims 2-4 are patentable for at least the same reasons as their respective independent claims, as well as for further patentable features recited therein.

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check or credit card payment form being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

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